Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	TI-25995
First Named Inventor or Application Identifier	Daniel J. Morgan, et al.
Title	Boundary Dispersion For Mitigating PWM Temporal Contouring Artifacts In Digital Displays
Express Mail Label No.	EM 008142680 US

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents

1. [+] *Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [+] Specification *[Total Pages* [18] *]* *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Bnef Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [+] Drawing(s) *(35 USC d113)* *[Total Sheets* [4] *]*
4. Oath or Declaration *[Total Pages* [1] *]*
   - a. [+] Newly Executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR §1 63(d)) *(for continuation/divisional with Box 17 completed)*

   [Note Box 5 below]

   - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §1 63(d)(2) and 1 33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identical of above copies

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & Documents(s))
9. [ ] 37 CFR §3 73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [+] Preliminary Amendment
13. [+] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] *Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *if foreign priority is claimed)*
16. [ ] Other

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: / .

Prior application information: ***Examiner*** _____ ***Group / Art Unit:*** _____

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [X] *Correspondence address below*

NAME	Julie L. Reed Texas Instruments Incorporated				
ADDRESS	P.O. Box 655474, MS 3999				
CITY	Dallas	STATE	Texas	ZIP CODE	75265
COUNTRY	USA	TELEPHONE	972-509-2844	FAX	972-917-4418

Name (Print/Type)	Julie L. Reed	Registration No. (Attorney/Agent)	35,349
Signature	Julie L. Reed	Date	6-2-98

PTO/SB/17 (1/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT	($) 790.00

Complete If Known	
Application Number	**Provisional 60/048,588**
Filing Date	**Provisional 06/04/97**
First Named Inventor	**Daniel J. Morgan, et al.**
Examiner Name	**TBD**
Group / Art Unit	**TBD**
Attorney Docket No.	**TI-25995**

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge to the following Deposit Account,

Deposit Account Number: 20-0668

Deposit Account Name: Texas Instruments Incorporated

☒ Charge any additional fee required or credit any overpayment

☐ Charge all indicated fees and any additional fee required or credit any overpayment

2. ☐ **Payment Enclosed:**

☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	$790
106	330	206	165	Design filing fee	$
107	540	207	270	Plant filing fee	$
108	790	208	395	Reissue filing fee	$
114	150	214	75	Provisional filing fee	$
				SUBTOTAL (1)	($)790

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	10	-20**=	0	x	22	=	0
Independent Claims	2	-3** =	0	x	82	=	0
Multiple Dependent						=	

**or number previously paid, if greater; For Reissue, see below

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent Claims in excess of 3
104	270	204	135	Multiple dependent claims in excess of 3
109	82	209	41	**Reissue independent claims over original patent
110	22	210	11	**Reissue claims in excess of 20 and over original patent
				SUBTOTAL (2) ($)0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension of time within second month	
117	950	217	475	Extension of time within third month	
118	1,510	218	755	Extension of time within fourth month	
128	2,060	228	1,030	Extension of time within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a bnef in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a pubic use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt.	
581	40	581	40	Recording each patent assignment per property (time number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1 129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) 0

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	Julie L. Reed			Reg. Number	35,349
Signature	Julie L Reed	Date	6-2-98	Deposit Account User ID	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Daniel J. Morgan	Docket:	TI-25995
Prov. Serial No.:	60/048,588	Examiner:	TBD
Serial No.:	TBD	Art Unit:	TBD
Prov. Filing Date:	06/04/97		
Filing Date:	Herewith		

For: Boundary Dispersion for Mitigation PWM Temporal Contouring Artifacts in Digital Displays

PRELIMINARY AMENDMENT

June 2, 1998

Assistant Commissioner
For Patents
Washington, D.C. 20231

Dear Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on the date below.

Denise Hill — 6-2-98
Denise Hill — Date

Please enter the following amendment prior to examination of the above-identified application.

IN THE SPECIFICATION:

Please amend the specification by inserting before the first line of the sentence

--This application claims priority under 35 U.S.C. §119 (c)(1) of provisional application Serial No. 60/048,588, filed on June 4, 1998. --

REMARKS

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicants.

Respectfully submitted,

Julie L Reed
Julie L. Reed
Reg. No. 35,349
Attorney for Applicants

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, Texas 75265
Telephone: (972) 509-2844
Facsimile: (972) 917-4418

BOUNDARY DISPERSION FOR MITIGATING PWM TEMPORAL CONTOURING ARTIFACTS IN DIGITAL DISPLAYS

Cross Reference to Related Applications:

Cross reference is made to the following co-pending patent applications, each being assigned to the same assignee as the present invention and the teachings included herein by reference:

SERIAL NUMBER	TITLE	FILING DATE
08/725,719	METHOD TO REDUCE PERCEPTUAL CONTOURING IN DISPLAY SYSTEMS	10-4-96
TI-25996 (Attorney's Docket #)	GLOBAL LIGHT BOOST FOR PULSE WIDTH MODULATION DISPLAY SYSTEMS	HEREWITH

FIELD OF THE INVENTION

The present invention relates generally to digital video display systems, and more particularly to digital display systems utilizing bit-planes for performing pulse width modulation to display digital video data.

BACKGROUND OF THE INVENTION

Binary spatial light modulators are typically comprised of an array of elements each having two states, on and off. The use of pulse width modulation (PWM) is one conventional approach of digitally displaying incoming analog video data, as compared to an analog display such as a cathode ray tube (CRT) based system. PWM typically comprises dividing a frame of incoming video data into weighted segments. For example, for a system that samples the luminance component of incoming video data in 8-bit samples, the video frame time is divided up into 255 time segments or pixel values (2^8-1). Conventionally, the 8-bit samples are formatted with binary values. The most significant bit (MSB) data is displayed on a given element for 128 time segments. In the present example, the

next MSB has a time period of 64 time segments, and so on, such that the next bits have weights of 32, 16, 8, 4, 2 and 1 time segments, consecutively. Thus, the least significant bit (LSB) has only one time segment. All pixel values are comprised of a summation of these weighted bits.

In DMD display systems, such as disclosed in commonly assigned U.S. Patent 5,278,652 entitled "DMD Architecture and Timing for Use in a Pulse-Width Modulated Display System", the teachings of which are incorporated herein by reference, light intensity for each pixel is typically displayed as a linear function of the pixel digital codes. For an 8-bit binary code, 0 is no light, 255 is peak light, and 128 is midscale light. Codes between 0 and 255 form a grayscale in each color. This grayscale sets the image resolution for the system by defining the number of discrete levels of light that can be produced for each color; i.e. red, green and blue. Pulse width modulation (PWM) schemes used to control the mirrors conventionally modulate the mirrors using bit-planes having weights based on powers of two. For example, 20 us, 40 us, 80 us, 160 us, 320 us, 640 us, 1280 us, and 2,560 us are used to define the mirror on-times for the 8 bit-planes needed for 8-bit video where 5.5 ms is available per color. Light is transmitted to the display screen as black for the bit-plane of a pixel which is logic 0 or at full brightness during a bit-plane which logic 1. Since the on-times for bit-planes vary, this results in PWM over a frame period. The viewer's eyes integrate the modulated light so that gray levels are formed and perceived.

A problem arises when using the PWM technique because the light is displayed in series of discrete burst during each frame. The shifts in ordering of these discrete bursts, as the displayed graycodes vary, generate artifacts in some images. For adjacent pixels, where major bit transitions take place, the sudden change in the ordering (and therefore time phase) of the discrete light burst within a frame causes noticeable pulsations in images upon viewing. Viewer's eyes integrate the out of phase ordering of mirror modulation, for adjacent pixels, to create the pulsations. These pulsations are referred to as PWM temporal contouring (hereafter referred to as simply PWM contouring), shown in Figure 1

because they create apparent contours in images that are time-varying. In commonly assigned U. S. Patent 5,619,228 entitled "Method for Reducing Temporal Artifacts in Digital Video Systems", there is disclosed one method of mitigating PWM contouring, the teachings of which are incorporated herein by reference.

PWM contouring can most clearly be seen on a grayscale ramp that goes horizontally across the screen. Here, vertical pulsations are seen at many major bit transitions when a viewer's eyes are scanned horizontally across the screen. When a viewer's eyes scan, the eyes integrate light only briefly over any given part of the screen. The viewer's scanning eyes catch the transmitted light for adjacent pixels out of time phase and pulsations are seen on the screen.

At normal viewing distance, PWM contouring for two adjacent pixels is difficult or impossible to resolve. However, in real images, boundary conditions often exists where many pixels are spatially bunched together with codes near each other (a sky scene for example). If these codes have clusters that cross a major bit transition, while others don't, PWM contouring will occur.

It is desirable to display data on a digital display, such as a DMD, with reduced PWM contouring artifacts without increasing system bandwidth.

SUMMARY OF THE INVENTION

The present invention achieves technical advantages by using boundary dispersion to selectively offset nominal pixel values alternately between a positive offset and a negative offset, repeatedly over a sequence of 2 displayed frames, whereby the average value of the two offset values over 2 displayed frames, as seen by the viewer, is equal to the nominal pixel value. For purpose of clarity the two frame sequence described below refers to two subsequent frames of source video data; however, the sequence can also be comprised of subframes within one frame of source video data. The chosen offset varies as a function of the nominal pixel value, the pixel spatial location on the screen, and pixel temporal location in time. The set of offsets is applied to pixel values is varied over a repeating 2-

frame sequence. Selected offsets are applied to pixel values within each frame as a function of spatial location on the DMD, and which of the 2 frames is being displayed. Within one frame, any given pixel value is offset by some amount above its correct value, and offset the same amount below its normal value in the next frame. Alternatively, the given pixel value is offset below its normal value in the first frame, and then offset above its normal value in the next frame. In either case, the average pixel value over the 2 frames, as perceived by the viewer, is equal to the nominal pixel value. The same is true of all pixels displayed on the DMD where an offset is used.

Boundary dispersion offsets certain pixel values from their nominal values in each frame according to preplanned spatial patterns. The spatial pattern used is dependent upon the value of the pixel codes. In each spatial pattern, some pixel values get a positive offset and some get a negative offset. In the next frame, an inverse set of offsets are used so that all pixels average to their nominal values over the consecutive 2-frame sequence.

A cluster of pixel codes at or near the transition of a major bit (e.g.8,16,32,64,128) use the offsets so that some pixels have a major bit set, and some without. Adjacent clusters of pixels, where one cluster contains pixels below the major bit and others contain pixels above the major bit, have the bit transition boundary dispersed. PWM contouring reduction is the result. The offsetting of some pixels positive and some negative in any given frame according to the spatial pattern also prevents any potential flicker artifacts that may be introduced by offsetting pixel codes over 2 frames.

A checkerboard pattern for a 2-frame sequence is one predefined pattern used to a disperse bit transition spatially around a bit transition boundary, for instance, the bit B5, which corresponds to the value of 32. Areas of the screen around this bit transition, for instance, codes 26 through 29, use more complex 2-frame patterns. The added complexity of these patterns is needed to control the density of pixels that have a major bit, i.e. B5, set in any given frame. A balance is struck between reducing PWM boundary artifacts and new artifacts introduced

within a spatial area having a given code. This is because if to many (or to few) pixels have the major bits set, i.e. B5, within an area using a given code, temporal noise can result in this area. The patterns are properly defined so that the contouring artifacts within a code (intra-code) are much less objectionable than the major bit transition boundaries (inter-code boundaries). By use of a particular pattern, for instance the checkerboard pattern, the spatial patterns have pixels with and without the major bits set are packed so spatially tightly that the intra-code contouring is not resolvable by a viewer at normal viewing distance. Since the PWM contouring is dispersed over a larger area, the overall temporal artifacts seen in the image are greatly reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an illustration of the source of PWM temporal contouring;

Figure 2 is an illustration of the PWM temporal contouring reduction using boundary dispersion according to the preferred embodiment of the present invention, whereby a checkerboard pattern is utilized to disperse a major bit transition, such as the B5 bit transition, spatially around the major bit transition boundary;

Figure 3 is an illustration of an adaptive version of the algorithm of the present invention that employs spatial patterns at and near areas of the screen having major bit transitions, whereby large clusters of pixel values interface one another along a boundary; and

Figure 4 shows a block diagram for implementing boundary dispersion logic according to the present invention, the boundary dispersion being performed by spatially identifying pixels on the DMD based on row and column, as well as identifying which frame of the 2-frame temporal sequence the pixel value is associated with, i.e. frame 1 or frame 2, whereby the correct offset is added or subtracted to each pixel value in a particular spatial-temporal assignment.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to Figure 2, there is illustrated PWM temporal contouring reduction using boundary dispersion according to the preferred embodiment of the present invention. Many of the pixel code values input to the DMD formatting electronics results in this value being offset from its nominal value when displayed on the DMD. The offset varies as a function of the pixel digital code, the pixel spatial location on the screen, and pixel temporal location in time. The set of offsets applied to pixel values is varied over a repeating 2-frame sequence. Selected offsets are applied to pixels within each frame as a function of spatial location on the DMD and which of the 2 frames are being displayed.

Within one frame, any given pixel is offset by some amount above or below its correct value, and offset below or above, respectively, its normal value in the next frame. The average value over the 2 frames, as seen by the viewer, is equal to the nominal pixel value. The same is true of all pixels displayed on the DMD where an offset is used.

Boundary dispersion offsets pixels from their nominal values in each frame according to preplanned spatial patterns. This spatial pattern used is dependent on the value of the pixel code to disperse the pixels that have a major bit transition. In each spatial pattern, some pixels get a positive offset and some get a negative offset. In the next frame, an inverse set of offsets are used so that all pixels average to their nominal value.

A cluster of pixel codes at or near the transition of a major bit (e.g.8, 16, 32, 64, 128) will have some pixels with this major bit set, and some without. Adjacent clusters of pixels, where one cluster contains pixel values below the major bit and the other cluster contains pixel values above the major bit have the bit transition boundary dispersed. PWM contouring reduction is the result.

As shown in Figure 2, there is illustrated spatial patterns implementing boundary dispersion, shown at top for areas of the screen using code 31 or code 32. A 2-frame checkerboard pattern is used to disperse the B5 bit transition spatially around the bit transition boundary. Areas of the screen having codes 26 - 29 use

more complex 2-frame patterns, shown in the middle checkerboard pattern. The added complexity of these patterns is needed to control the density of pixels that have B5 set in any given frame. A balance is struck between reducing PWM boundary artifacts and the new artifacts introduced within a spatial area having a given code. If to many (or to few) pixels have B5 set, within an area using a given code, temporal noise can result in this area. This temporal noise is actually a form of PWM contouring, except now the contouring occurs on the screen within areas having the same pixel codes, rather than at major bit boundaries between clusters of pixels on the screen.

Since the patterns are properly defined, the contouring artifacts within a code (intra-code) are much less objectionable than at major bit transition boundaries (inter-code). In fact, for most patterns (like the checkerboard pattern) the spatial patterns having the pixels with and without the major bit set are packed so tightly that the intra-code contouring is not resolvable by a viewer at normal viewing distance. The fact that adjacent pixels have transmitted light out of time phase cannot be resolved.

As illustrated in Figure 2, the transition between codes 31 and 32 have the PWM contouring at this boundary dispersed to within codes 31 and 32 rather than having a clearly defined boundary. Since the PWM contouring is dispersed over a larger area, the overall temporal artifacts seen in the image are greatly reduced.

Figure 3 illustrates an adaptive version of the algorithm that only employs the spatial patterns at and near areas of the screen having major bit transitions. This approach allows for any intra-code artifacts created by the present invention to be eliminated for areas of the screen not needing boundary dispersion invoked.

Referring back to Figure 2, it can be seen that for other pixel values further away from the transition boundary, such as pixel values 26, 27, 28 and 29, using boundary dispersion sets the major bit during one frame, but not the next frame to help control the density of pixels that have B5 set in any given frame. For a pixel code of 29, for instance, a pixel code of 33 (29 + 4) is displayed during frame 1, with a pixel code of 25 (29 - 4) being displayed the frame 2. For a pixel code of

27, a pixel code of 33 (27 + 6) is displayed the first frame, with a pixel code of 21 (27 - 6) being displayed the next frame. Thus, a major bit is set one frame, but not the next.

As shown in Figure 2, the checkerboard pattern takes into account the spatial location of the pixels in the display. For instance, for a pixel identified at 20 in column 1, row 1, the lower value is displayed during frame 1, and the higher value being displayed in frame 2. For an adjacent pixel such as the pixel identified at 22, being in row 1 column 2, the higher value is displayed during frame 1 and the lower value being displayed frame 2. Again, the average over this 2-frame sequence is the nominal pixel value.

Still referring to Figure 2, to display a pixel value of 28, for instance, 25% of the pixels are set up to use the MSB B5. As shown, every other row of pixels utilizes the MSB B5 in one frame, and not the next. In row 2 and row 4, for instance, the MSB is never used, although the pixel value is offset a lower amount i.e. +/- 2, for these rows to help minimize temporal contouring. For instance, pixel 24 will have a value of 30 during frame 1, and 26 the next frame. The adjacent pixel in row 2 column 2, however, will have the lower value of 26 during frame 1 and the higher value of 30 the next frame. In either instance, pixel 24 never has the MSB B5 set. The MSB is only set in the odd rows of pixels for pixel values that are closer to a bit transition, i.e. 26, 27, 28, and 29.

For even lower values of pixel codes that are further away from a bit transition, i.e. pixel codes 24 and 25, none of the pixels use the MSB B5, however, the value of the pixel code is dithered from frame to frame slightly, i.e. + or - 2, to help achieve acceptable temporal contouring mitigation.

Referring again to Figure 3, there is shown how a section or cluster of pixels are displayed as a function of the source pixels for the same cluster. If there is a boundary defined by a cluster of pixel values i.e. 29 and 30, using the boundary dispersion process of the present invention the pixel values of 30 will be either +2 or -2, depending on the frame being displayed. However, the pixel values of 29 will be offset either +4 or -4, depending upon the frame being displayed. Again,

this allows the MSB B5 to be displayed, in this case 50% of the time. Figure 3 illustrates the algorithm whereby for a pixel "N", if any of the 24 neighbors of pixel N (P1-P24) have an MSB transition, the boundary dispersion is performed on pixel N to achieve PWM temporal contouring.

Referring now to Table 1 below, there is shown one preferred approach of providing boundary dispersion for the whole set of pixel codes between 0 and 255 to help disperse a major bit transition spatially around the bit transition boundaries.

TABLE 1

Code	Offsets	Pattern Type
255	+/-0	None
254	+/-0	None
253	+/-2	Checkerboard
252	+/-2	Checkerboard
251	+/-2	Checkerboard
250	+/-2	Checkerboard
249	+/-2	Checkerboard
248	+/-2	Checkerboard
247	+/-2	Checkerboard
246	+/-2	Checkerboard
245	+/-6,+/-2	25% Crossing
244	+/-6,+/-2	25% Crossing
243	+/-4,+/-2	25% Crossing
242	+/-4,+/-2	25% Crossing
241	+/-2	Checkerboard
240	+/-2	Checkerboard
239	+/-2	Checkerboard
238	+/-2	Checkerboard
237	+/-4,+/-2	25% Crossing
236	+/-4,+/-2	25% Crossing
235	+/-6,+/-2	25% Crossing
234	+/-6,+/-2	25% Crossing
233	+/-2	Checkerboard
232	+/-2	Checkerboard
.		
.		
.		
73	+/-2	Checkerboard
72	+/-2	Checkerboard
71	+/-2	Checkerboard
70	+/-2	Checkerboard
69	+/-6,+/-2	25% Crossing
68	+/-6,+/-2	25% Crossing

67	+/-4,+/-2	25% Crossing
66	+/-4,+/-2	25% Crossing
65	+/-2	Checkerboard
64	+/-2	Checkerboard
63	+/-2	Checkerboard
62	+/-2	Checkerboard
61	+/-4,+/-2	25% Crossing
60	+/-4,+/-2	25% Crossing
59	+/-6,+/-2	25% Crossing
58	+/-6,+/-2	25% Crossing
57	+/-2	Checkerboard
56	+/-2	Checkerboard
55	+/-2	Checkerboard
54	+/-2	Checkerboard
53	+/-6,+/-2	25% Crossing
52	+/-6,+/-2	25% Crossing
51	+/-4,+/-2	25% Crossing
50	+/-4,+/-2	25% Crossing
49	+/-2	Checkerboard
48	+/-2	Checkerboard
47	+/-2	Checkerboard
46	+/-2	Checkerboard
45	+/-4,+/-2	25% Crossing
44	+/-4,+/-2	25% Crossing
43	+/-6,+/-2	25% Crossing
42	+/-6,+/-2	25% Crossing
41	+/-2	Checkerboard
40	+/-2	Checkerboard
39	+/-2	Checkerboard
38	+/-2	Checkerboard
37	+/-6,+/-2	25% Crossing
36	+/-6,+/-2	25% Crossing
35	+/-4,+/-2	25% Crossing
34	+/-4,+/-2	25% Crossing
33	+/-2	Checkerboard
32	+/-2	Checkerboard
31	+/-2	Checkerboard
30	+/-2	Checkerboard
29	+/-4,+/-2	25% Crossing
28	+/-4,+/-2	25% Crossing
27	+/-6,+/-2	25% Crossing
26	+/-6,+/-2	25% Crossing
25	+/-2	Checkerboard
24	+/-2	Checkerboard
23	+/-2	Checkerboard
22	+/-2	Checkerboard
21	+/-6,+/-2	25% Crossing
20	+/-6,+/-2	25% Crossing
19	+/-4,+/-2	25% Crossing
18	+/-4,+/-2	25% Crossing

17	+/-2	Checkerboard
16	+/-2	Checkerboard
15	+/-2	Checkerboard
14	+/-2	Checkerboard
13	+/-2	Checkerboard
12	+/-2	Checkerboard
11	+/-2	Checkerboard
10	+/-2	Checkerboard
9	+/-2	Checkerboard
8	+/-2	Checkerboard
7	+/-2	Checkerboard
6	+/-2	Checkerboard
5	+/-0	None
4	+/-0	None
3	+/-0	None
2	+/-0	None
1	+/-0	None
0	+/-0	None

The larger the pixel value, the more pixel codes adjacent this boundary that have temporal contouring applied.

Referring now to Figure 4, there is shown a block diagram of the present invention. 24-bit data (8 bits per color) is the input from the video source. A degamma function 30 is applied to each RGB color so that the DMD display output matches a CRT response. Since the degamma output is limited to 24 bits, a spatial contouring filter is included that diffuses the 8-bit per color quantization errors for low intensity pixels. The boundary dispersion logic 32 according to the present invention accepts the spatial contouring filter output. The boundary dispersion logic 32 receives signals to identify pixels spatially on the DMD, which signals are provided on signal lines row count ROWCNT and column count COLUMNCNT. A signal is also provided to identify the particular frame of the 2-frame temporal sequence, identified as signal FRAME 1/2. A logic high on this line indicates a FRAME 1, and a logic 0 indicates FRAME 2. The boundary dispersion logic assigns spatial patterns as a function of these signals where offsets are applied to each 8-bit color pixel. The offset values are provided to the boundary dispersion logic 32 so that the correct offset is added or subtracted to each pixel in a particular spatial-temporal assignment, as shown in Figure 2 and illustrated in Table 1. The offsets and spatial-temporal patterns applied by the boundary dispersion logic 32 are also a function of the pixel codes. Table 1 illustrates this. Figure 2 illustrates how the boundary dispersion logic is applied to pixels in a spatial-temporal manner.

The 24 signals from the boundary dispersion logic 32 are input into the DMD data formatting logic 40. The DMD data formatting logic organizes the input data into words which form digital planes of information and then loads them into banks of RAM 42. Data is written to one bank of RAM 40 while the other bank is being continuously read and written to the DMD. Thus, a double-buffer memory is used. The buffers are swapped at each VSYNC which indicates a frame boundary for source pixels.

TABLE 2

	PIXEL VALUE	plus					minus					w/GB +/-	no GB +/-
0000	16	2					2						2
0001	17	4	7	8			8	7	5	4			2
0010	18	1	2	4	5		4						4
0011	19	2	5	6			5						4
0100	20	6					6						6
0101	21	8	11	12			12	11	9	8			6
0110	22	5	6	8	9		8						8
0111	23	6	9	10			9						8
1000	24	5	8	9			9	8	5				8
1001	25	4	7	8			8	7	5	4			8
1010	26	8					9	8	6	5			6
1011	27	2	5	6			5						6
1100	28	1	4	5			5	4	1				4
1101	29	0	3	4			4	3	1	0			4
1110	30	4					5	4	2	1			2
1111	31	-2	1	2			1						2

Referring now to Table 2, there is shown an alternative embodiment of the present invention to account for any problems that may occur when boundary dispersion according to the present invention is utilized in combination with a global boost algorithm, as disclosed in commonly assigned patent application identified as Attorney's Docket TI-25996 entitled "GLOBAL LIGHT BOOST FOR PULSE WIDTH MODULATION DISPLAY SYSTEMS" filed herewith, and the teachings of which are incorporated herein by reference.

An example of a problem occurs when boundary dispersion receives an input pixel value of 17. The boundary dispersion algorithm may perform a +/-2 offset on the 17 and output a 19 one frame and a 15 the other frame according to a checkerboard pattern to traverse the PWM bit boundary. The global boost algorithm, as disclosed in the co-pending patent application, then outputs a (16,16+6) pattern for the 19 value, and a (8+6,16) pattern for the 15 value. The problem is that the output will be (16,16) or (16+6, 8+6) depending upon the phase relationship between the boundary dispersion and the global boost checkerboards. These two patterns yield DC PWM output of (16+16)/2=16 or (22+14)/2+18 depending upon the phase. If it is 16, the output DC PWM has an error of -1 since it should be 17. Furthermore, a DC value of 1 cannot simply be added in global boost or boundary dispersion to offset this error because the result of the +1 will yield other checkerboard conflicts, as well. Note that Table 2, which illustrates codes 16-31 may be repeated to all 256 grayshades.

Though the invention has been described with respect to a specific preferred embodiment, many variations and modifications will become apparent to those skilled in the art upon reading the present application. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.

WE CLAIM

1. A method of displaying digital video data comprising pixel values using pulse width modulation, comprising the steps of:

offsetting a first said pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and

offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

2. The method as specified in Claim 1 wherein the value of said first predetermined amount is selected as a function of said first pixel value.

3. The method as specified in Claim 1 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

4. The method as specified in Claim 1 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

5. The method as specified in Claim 1 wherein said first display frame and said second display frame are consecutive.

6. A system of displaying digital video data comprising pixel values using pulse width modulation, comprising:

a logic circuit offsetting a first said pixel value a first predetermined amount to form a first offset pixel value said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and

display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

7. The system as specified in Claim 6 wherein the value of said first predetermined amount is selected by said logic circuit as a function of said first pixel value.

8. The system as specified in Claim 6 wherein said first offset pixel value is greater than or less than said first pixel value as a function of the spatial location that said first pixel value is to be displayed.

9. The system as specified in Claim 6 wherein said pixel values are displayed using a plurality of weighted bit-planes, wherein said first pixel values close to a bit transition of said bit-planes are offset during said first display frame and said second display frame.

10. The system as specified in Claim 6 wherein said first display frame and said second display frame are consecutive.

ABSTRACT

A method and system providing boundary dispersion to pixel values displayed on a binary spatial light modulator to reduce temporal contouring artifacts. Pixel code values are offset from a nominal value when displayed on the SLM to disperse a large bit transition for a pulse width modulation (PWM) system. The offset value varies as a function of the pixel digital code, the pixel spatial location on the screen, and pixel temporal location in time. The set of offsets applied to pixels is varied over a repeating sequence of 2 displayed frames.

ATTORNEY'S DOCKET NO
TI-25995

APPLICATION FOR UNITED STATES PATENT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, section 1.56(a);

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION: **BOUNDARY DISPERSION FOR MITIGATING PWM TEMPORAL CONTOURING ARTIFACTS IN DIGITAL DISPLAYS**		
POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH Robert C. Klinger, Reg. No. 34,365 James C. Kesterson, Reg. No. 25,882 Richard L. Donaldson, Reg. No. 25,673 John D. Kaufmann, Reg. No. 24,017 William B. Kempler, Reg. No. 28,228 Jay Cantor, Reg. No. 19,906		
SEND CORRESPONDENCE TO: Robert C. Klinger, Texas Instruments Incorporated, P. O. Box 655474, M/S 219 Dallas, Texas 75265		DIRECT TELEPHONE CALLS TO: Robert C. Klinger (972) 995-3516
NAME OF INVENTOR: (1) Daniel J. Morgan	NAME OF INVENTOR: (2) Gregory J. Hewlett	NAME OF INVENTOR: (3) Peter F. VanKessel
RESIDENCE (City and State Only) Denton, Texas	RESIDENCE (City and State Only) Garland, Texas	RESIDENCE (City and State Only) Allen, Texas
Post Office Address 2621 Woodhaven Denton, Texas 76201	Post Office Address 2831 North Shiloh Rd. #268 Garland, Texas 75044	Post Office Address 1311 San Mateo Dr. Allen, Texas 75013
COUNTRY OF CITIZENSHIP: U.S.A.	COUNTRY OF CITIZENSHIP: U.S.A.	COUNTRY OF CITIZENSHIP: U.S.A.
SIGNATURE OF INVENTOR: Daniel J. Morgan	SIGNATURE OF INVENTOR: Gregory J Hewlett	SIGNATURE OF INVENTOR: Peter F VanKessel
DATE: 6-10-97	DATE: 6-19-97	DATE: 6-11-97

FIG. 1

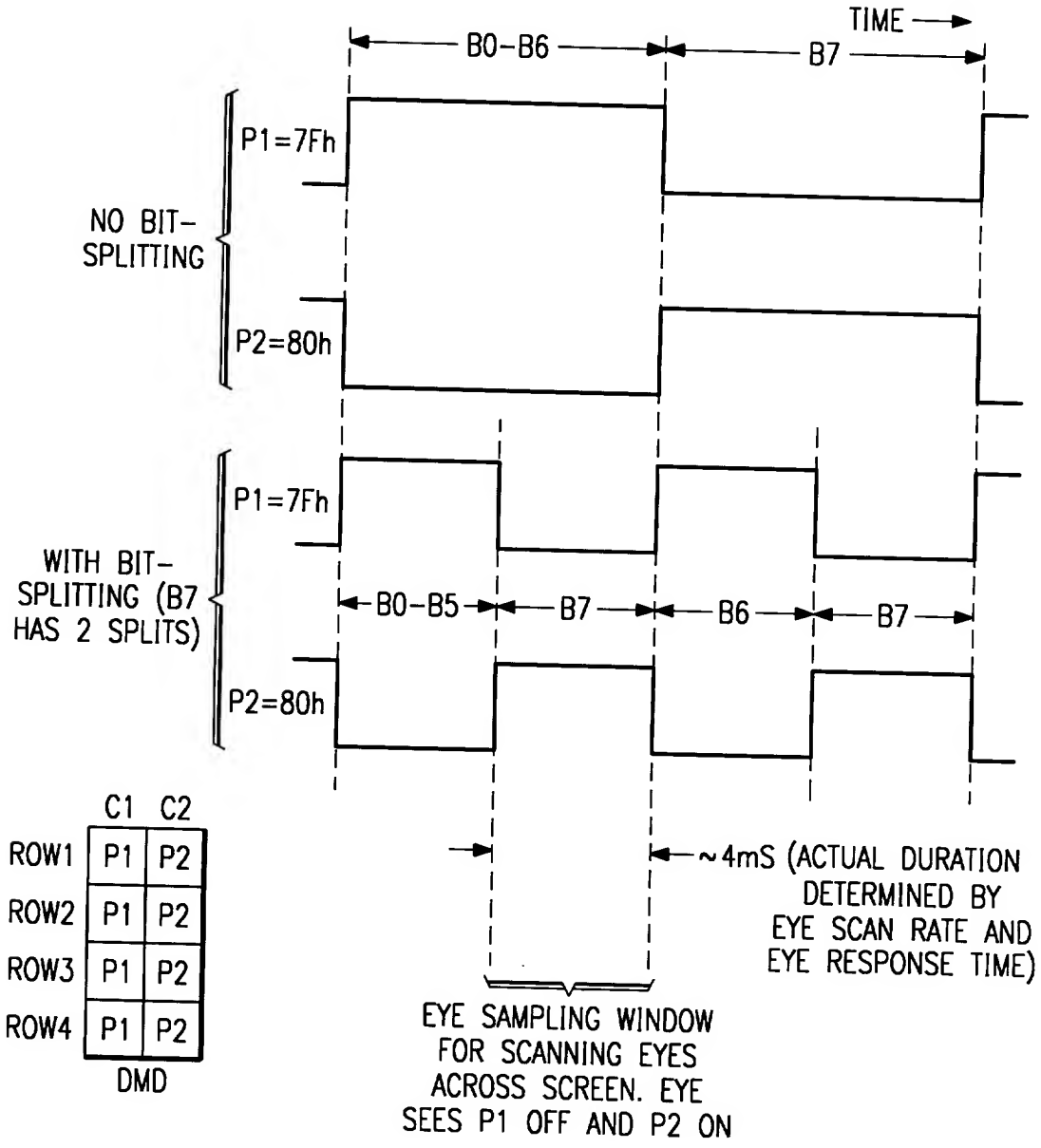
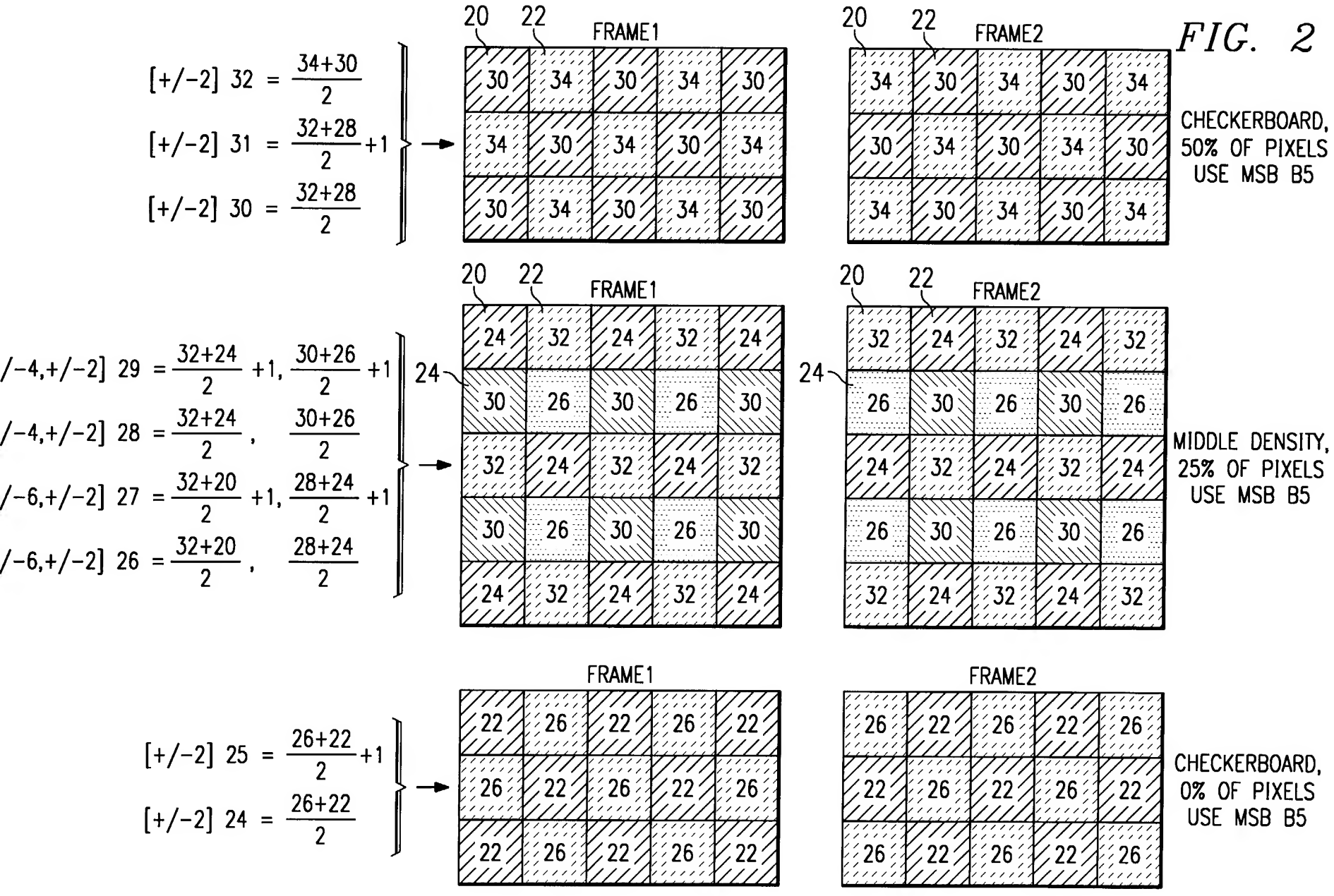

TIME
B0-B6
B7
P1=7Fh
NO BIT-SPLITTING
P2=80h
P1=7Fh
WITH BIT-SPLITTING (B7 HAS 2 SPLITS)
B0-B5
B7
B6
B7
P2=80h
C1 C2
ROW1 P1 P2
ROW2 P1 P2
ROW3 P1 P2
ROW4 P1 P2
DMD
~4mS (ACTUAL DURATION DETERMINED BY EYE SCAN RATE AND EYE RESPONSE TIME)
EYE SAMPLING WINDOW FOR SCANNING EYES ACROSS SCREEN. EYE SEES P1 OFF AND P2 ON

FIG. 2


[+/-2] 32 = (34+30)/2
[+/-2] 31 = (32+28)/2 +1
[+/-2] 30 = (32+28)/2
20
22
FRAME1
30 34 30 34 30
34 30 34 30 34
30 34 30 34 30
FRAME2
34 30 34 30 34
30 34 30 34 30
34 30 34 30 34
CHECKERBOARD, 50% OF PIXELS USE MSB B5
[+/-4,+/-2] 29 = (32+24)/2 +1, (30+26)/2 +1
[+/-4,+/-2] 28 = (32+24)/2, (30+26)/2
[+/-6,+/-2] 27 = (32+20)/2 +1, (28+24)/2 +1
[+/-6,+/-2] 26 = (32+20)/2, (28+24)/2
24
24 32 24 32 24
30 26 30 26 30
32 24 32 24 32
30 26 30 26 30
24 32 24 32 24
32 24 32 24 32
26 30 26 30 26
24 32 24 32 24
26 30 26 30 26
32 24 32 24 32
MIDDLE DENSITY, 25% OF PIXELS USE MSB B5
[+/-2] 25 = (26+22)/2 +1
[+/-2] 24 = (26+22)/2
22 26 22 26 22
26 22 26 22 26
22 26 22 26 22
26 22 26 22 26
22 26 22 26 22
26 22 26 22 26
CHECKERBOARD, 0% OF PIXELS USE MSB B5

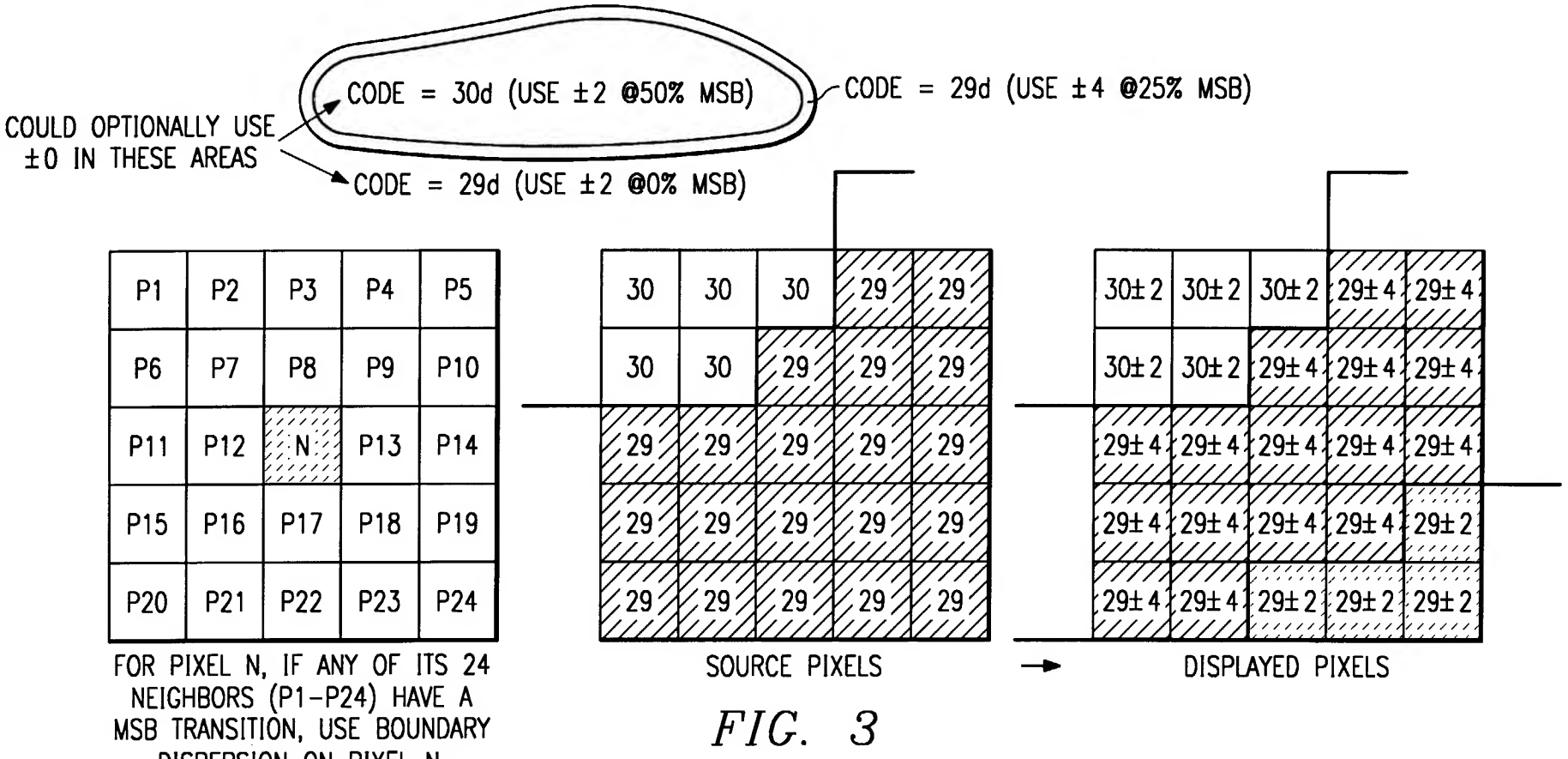

CODE = 30d (USE ±2 @50% MSB)
CODE = 29d (USE ±4 @25% MSB)
COULD OPTIONALLY USE ±0 IN THESE AREAS
CODE = 29d (USE ±2 @0% MSB)
P1 P2 P3 P4 P5
P6 P7 P8 P9 P10
P11 P12 N P13 P14
P15 P16 P17 P18 P19
P20 21 P22 P23 P24
30 30 30 29 29
30 30 29 29 29
29 29 29 29 29
29 29 29 29 29
29 29 29 29 29
30±2 30±2 30±2 29±4 29±4
30±2 30±2 29±4 29±4 29±4
29±4 29±4 29±4 29±4 29±4
29±4 29±4 29±4 29±4 29±2
29±4 29±4 29±2 29±2 29±2
FOR PIXEL N, IF ANY OF ITS 24 NEIGHBORS (P1–P24) HAVE A MSB TRANSITION, USE BOUNDARY DISPERSION ON PIXEL N.
SOURCE PIXELS
DISPLAYED PIXELS

FIG. 3

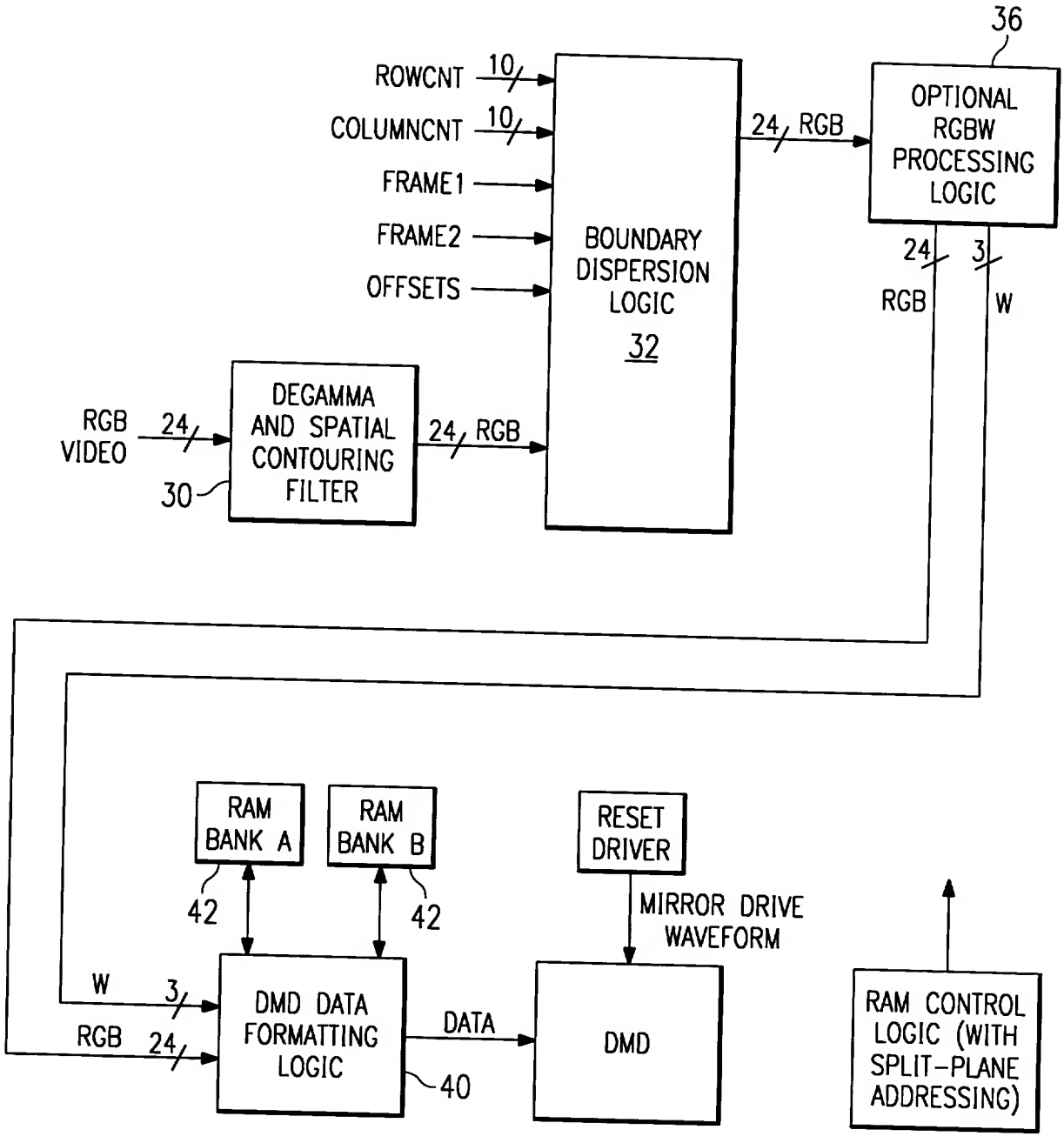

36
ROWCNT
10
COLUMNCNT
10
FRAME1
FRAME2
OFFSETS
BOUNDARY DISPERSION LOGIC
32
24 RGB
OPTIONAL RGBW PROCESSING LOGIC
24
RGB
3
W
RGB VIDEO
24
DEGAMMA AND SPATIAL CONTOURING FILTER
30
24 RGB
RAM BANK A
RAM BANK B
42
42
RESET DRIVER
MIRROR DRIVE WAVEFORM
W
3
RGB
24
DMD DATA FORMATTING LOGIC
40
DATA
DMD
RAM CONTROL LOGIC (WITH SPLIT-PLANE ADDRESSING)

FIG. 4